APRO Co., Ltd.

July 2010

Product Specification

Rugged Metal 2.5” SATA II MLC SSD supports DDRII SDRAM Cache

-HERMES-R Series-

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Revision History

Revision	Description	Date
1.0	Initial Release	2010/7/30

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1. Introduction

APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series provide high capacity flash memory Solid State Drive (SSD) that electrically complies with Serial ATA 2.6 (SATA) standard and supports SATA Gen-II (3.0 GB/s) with high performance. The main used flash memories are MLC-NAND type flash memory chips. The available disk capacities are 16GB, 32GB, 64GB, 128GB and 256GB.

The operating temperature grade is optional for commercial grade 0°C ~ 70°C and Industrial grade with special conformal coating treatment on PCBA completely which may support operating temperature -40°C ~ +85°C. The data transfer performance such like the 64GB SSD, the sequential read is up to 245.7MB/sec, and sequential write is up to 105.2 MB/sec.

The APRO Rugged Metal 2.5" SATA II MLC SSD built-in DDRII 512Mbits SDRAM products provide a high level interface to the host computer. It is native design to provide higher bandwidth for flash memory access. Each sector is protected by a powerful 16 bits / 24 bits error correction (ECC). APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the high tech Rugged Metal 2.5" SATA II MLC SSD in HERMES-R Series.

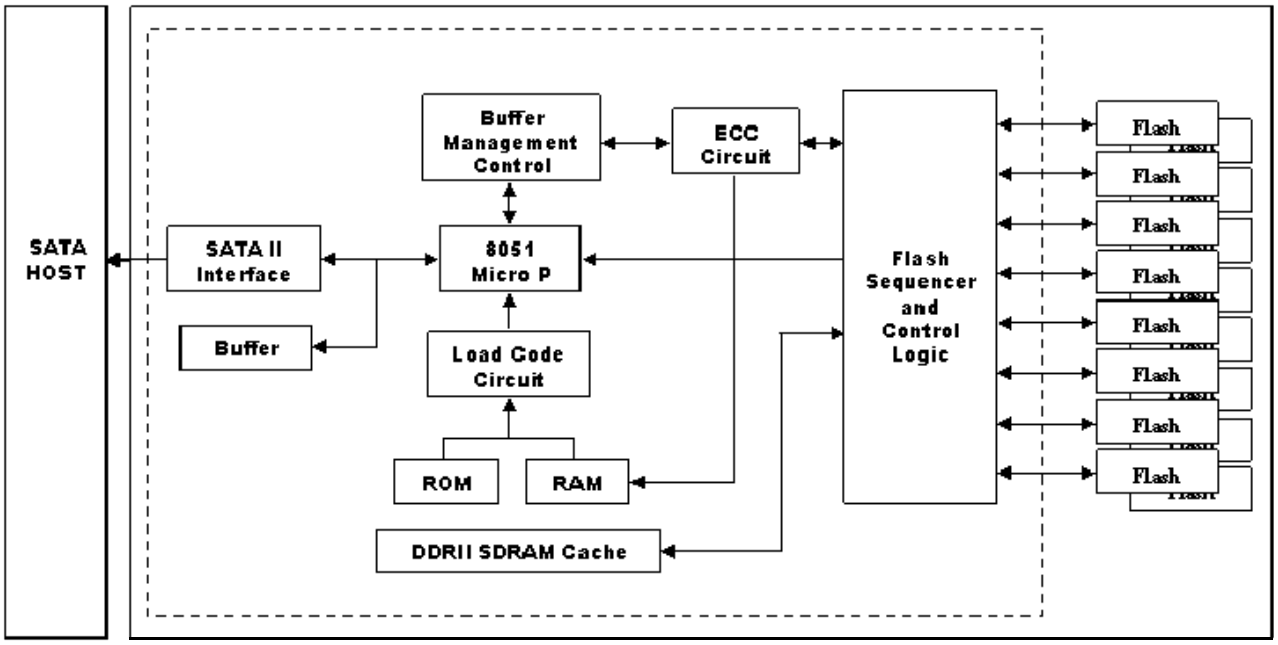

Figure 1: APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series system block diagram

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1.1. *Scope*

This document describes the features and specifications and installation guide of APRO's Rugged Metal 2.5" SATA II MLC SSDs – HERMES-R Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *System Features*

- MLC-NAND type flash technology
- Standard 2.5" SATA Flash Disk form-factor (9.5mm height)
- SATA 7-pin (data) + 15-pin (power connector) SATA Interface
- Extremely Rugged Metal casing to endure harsh environments
- SATA 1.0a and SATA 2.6 specification compliance
- SMART (Self-Monitoring, Analysis and Reporting Technology) function supported.
- Non-volatile memory and no moving parts
- MLC Flash SSD standard grade capacity from 16GB up to 256GB
- Sequential read performance up to 245.7MB/sec (8CH/64GB)
- Sequential write performance up to105.2 MB/sec (8CH/64GB)
- Automatic 16 bits or 24 bits error correction (ECC) and retry capabilities
- +5 V ±10% or +3.3 V ±5% operation
- Shock : 1,500G, compliance to MIL-STD-810F
- Vibration : 15G, compliance to MIL-STD-810F
- Very high performance, very low power consumption
- Low weight, Noiseless
- Commercial grade supports operating temperature 0°C to +70°C, and Industrial Grade, -40°C to +85°C with special conformal coating treatment on PCBA

1.3. *Flash Management Technology - Static Wear Leveling*

In order to gain the best management for flash memory, APRO 2.5" SATA II MLC SSD HERMES-R Series supports Static Wear-leveling technology to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

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1.4. *ECC Technology*

Please refer to Figure 2. Figure 2 is a diagram illustrating an allocation method of a spare area in each page of a NAND flash memory, wherein the specific ECC algorithm utilizes a Bose, Chaudhuri and Hocquengham (BCH) ECC algorithm. When a BCH 8 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 13 bytes of the spare area in each page. When a BCH 15 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 25 bytes of the spare in each page.

When a BCH 8 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in one sector (512 Bytes) is 8. When a BCH 15 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in one sector is 15.

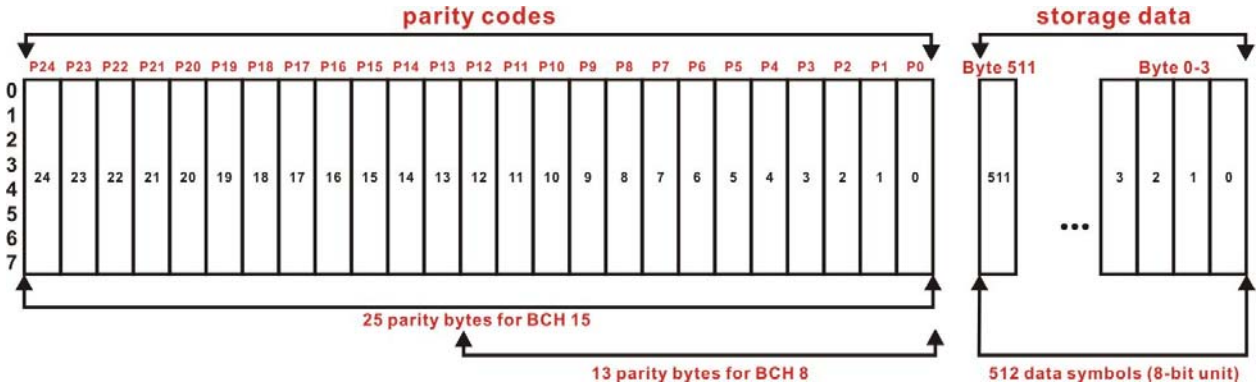

Figure 2: Allocation for ECC Algorithm BCH in NAND Flash

1.5. *Conformal Coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO apply MIL-I-46058C silicon conformal coating.

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1.6. *Bad Block Management*

Bad blocks of NAND flash may accumulate up to 2% of entire number of blocks during its manufacturing process and during the flash operational usage.

A system must be able to recognize bad block(s) based on the original bad block information and create a bad block table to keep track of blocks that fail during use. The first block of NAND Flash (block 0) is guaranteed to be good. The bad block information is stored in the reservoir area that is located in the highest address region of the NAND flash. Once the bad blocks have been located, and the bad blocks be no longer accessed.

To locate the bad blocks on a brand new device, read out each block. Any block that is not all FFFFh in 1st sector of 1st or 2nd page in a spare area is a bad block. Although random bit errors may occur during use, this does not necessarily mean that a block is bad. Generally, a block should be marked as bad only when there is a problem or erase failure. This can be determined by doing a status read after erase/program operation. The flash memory is initialized by formatting the flash memory into a reserved area and user area.

In order to detect the initial bad blocks to handle run time bad blocks, APRO HERMES Series' SSD provides the Bad Block Management scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

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2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series		Commercial Grade SR2SRxxxG-JDCMC	Industrial Grade WR2SRxxxG-JDCMC/C
Temperature	Operating: Non-operating:	0ºC ~ +70ºC -20ºC ~ +80ºC	-40ºC ~ +85ºC -50ºC ~ +95ºC
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
Vibration	Operating & Non-operating:	15G, compliance to MIL-STD-810F	
Shock	Operating & Non-operating:	1,500G, compliance to MIL-STD-810F	

2.2. System Power Requirements

Table 2: Power Requirement

APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series		Commercial Grade SR2SRxxxG-JDCMC	Industrial Grade WR2SRxxxG-JDCMC/C
DC Input Voltage (VCC) 100mV max. ripple(p-p)		5V±10% / 3.3V±5%	
+5V Current (Maximum average value)	Reading Mode :	430mA (max.)	
	Writing Mode :	490mA (max.)	
	Idle Mode :	260mA (max.)	

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting		Serial ATA Gen-II (3.0Gb/s = 380MB/s)				
Average Access Time		0.1 ms (estimated)				
Maximum Performance	Capacity	16GB	32GB	64GB	128GB	256GB
	Sequential Read (MB/s)	102.3	217	245.7	239.2	239.2
	Sequential Write(MB/s)	50.3	65	105.2	91.7	91.7
The number of Flash IC		8pcs	16pcs	16pcs	16pcs	16pcs

Note:

(1). All values quoted are typically at 25℃ and nominal supply voltage.

(2). Testing of the Rugged Metal 2.5" SATA II MLC SSD maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor

- Windows XP Professional operating system

(3). Above performance data are for reference only for the performance would be different for various factors such like flash memory chips, system configurations, OS and software for performance testing,…etc.

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Table 4: Small files data transfer performance by IOPS / Average I/O time / Average Performance testing

Data Transfer Size	IOPS / sec.		Average I/O time (ms)		Average Performance (MB/sec)	
	Read	Write	Read	Write	Read	Write
512 bytes	7138	7235	0.14	0.14	3.48	3.54
4 KB	4343	5372	0.23	0.19	16.96	20.98
64 KB	1990	1834	0.50	0.55	124.4	114.65
1 MB	197	81	5.1	12	197.3	81.23

2.4. *System Reliability*

Table 5: System Reliability

Wear-leveling Algorithms	Static Wear-leveling
Bad Blocks Management	Supportive
ECC Technology	Support BCH 16/24 bits ECC

2.5. *Physical Specifications*

Refer to Table 6 and see Figure 3 for Rugged Metal 2.5” SATA II MLC SSD HERMES-R Series physical specifications and dimensions.

Table 6: Physical Specifications of APRO Rugged Metal 2.5” SATA II MLC SSD HERMES-R Series

Length:	99.7 mm / 3.925 in
Width:	69.9 mm / 2.752 in
Thickness:	9.5 mm / 0.374 in
Weight:	115.00 g / 4.06 oz

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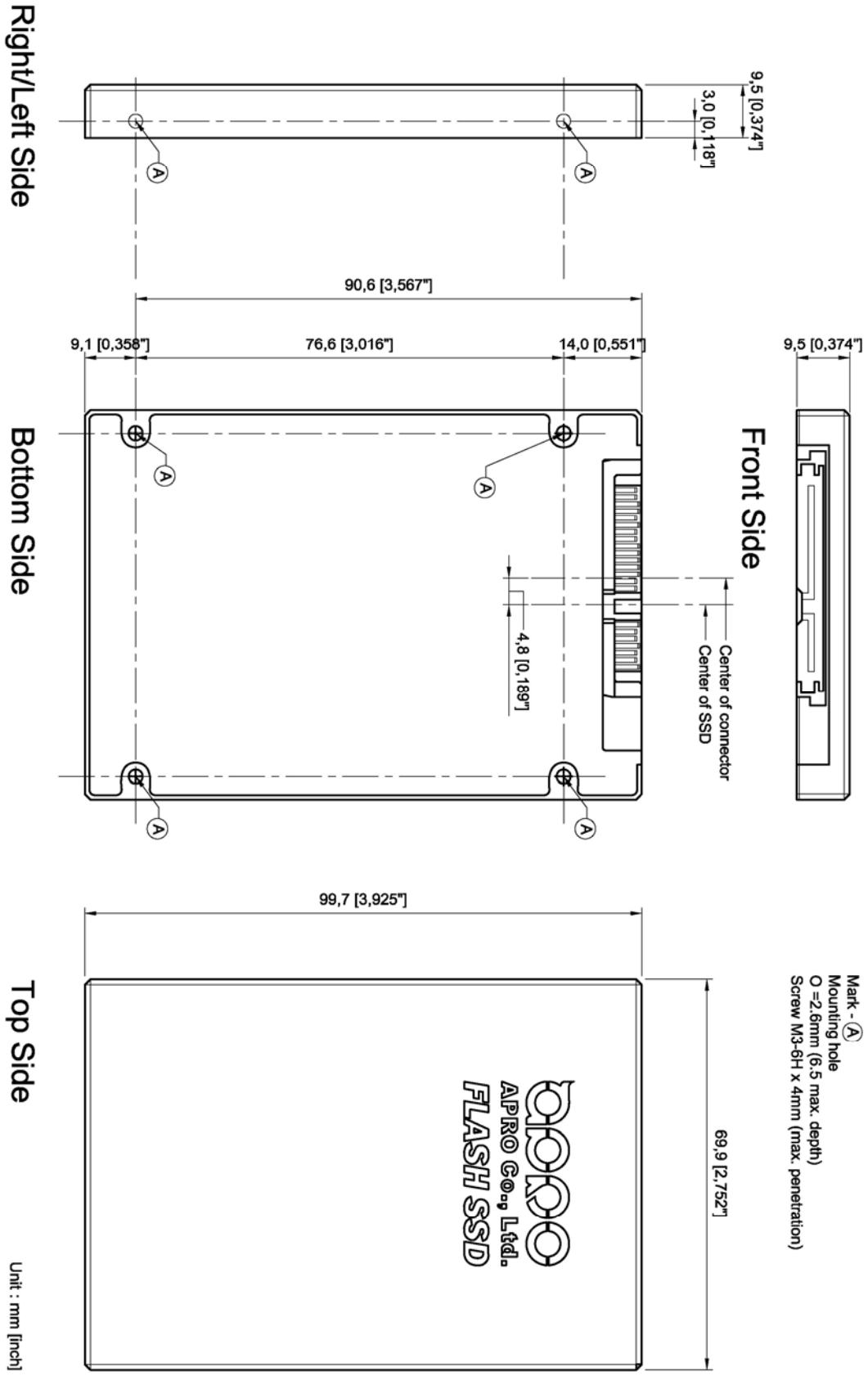

Figure 3: APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series Dimension

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2.6. *Capacity Specifications*

APRO Rugged Metal 2.5” SATA II MLC SSDs are built-in mainly MLC -NAND Type Flash memory chips. The Table 7 shows the part number of applied Flash memory chips for each card.

Table 7: Card Configuration vs. Samsung NAND MLC part number

Card capacity	Samsung MLC flash memory part number * Q’TY
16GB	K9GAG08U0M (16Gb) or equal * 8
32GB	K9LBG08U1M (32Gb) or equal * 8
64GB	K9LBG08U1M (32Gb) or equal * 16
128GB	K9HCG08U5M (64Gb) or equal * 16
256GB	K9MDG08U5M (128Gb) or equal * 16

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3. Interface Description

3.1. SATA II interface

APRO Rugged Metal 2.5” SATA II MLC SSD HERMES-R Series comes with 7 pins + 15 pins Serial ATA connector.

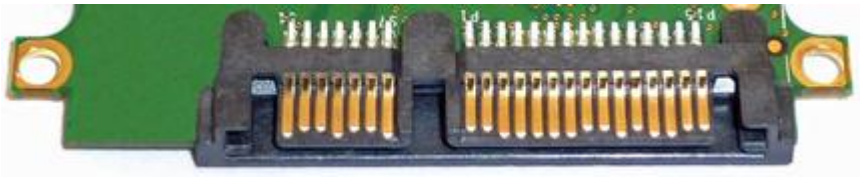

Figure 4: The connectors of 2.5” SATA II MLC SSD

3.2. Pin Assignments

There are total of 7 pins in the signal segment and 15 pins in the power segment. The pin assignments are listed in below table 8.

Table 8 - Pin Assignments

Name	Type	Description
S1	GND	
S2	A+	Differential Signal Pair A
S3	A-	
S4	GND	
S5	B-	Differential Signal Pair B
S6	B+	
S7	GND	

Key and Spacing separate signal and power segments		
P1	V33	3.3V Power
P2	V33	3.3V Power
P3	V33	3.3V Power, Pre-charge
P4	GND	
P5	GND	
P6	GND	
P7	V5	5V Power, Pre-Charge
P8	V5	5V Power
P9	V5	5V Power
P10	GND	

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Key and Spacing separate signal and power segments		
P11	DAS/DSS	Device Activity Signal / Disable Staggered Spin up
P12	GND	
P13	V12	12V Power, Pre-charge
P14	V12	12V Power
P15	V12	12V Power

Notes:

1. *All pins are in a signal row with a 1.27 mm (0.050" pitch).*
2. *The commands on the mating sequence in forward table apply to the case of backplane blind mate connector only. In this case, the mating sequences are:*
   (1) The pre-charge power pins and other ground pins.
   (2) The signal pins and the rest of the power pins.

3.3. *Out of bank signaling*

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 ALIGNP primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having duration of 160 UIOOB. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 5 and Table 9.

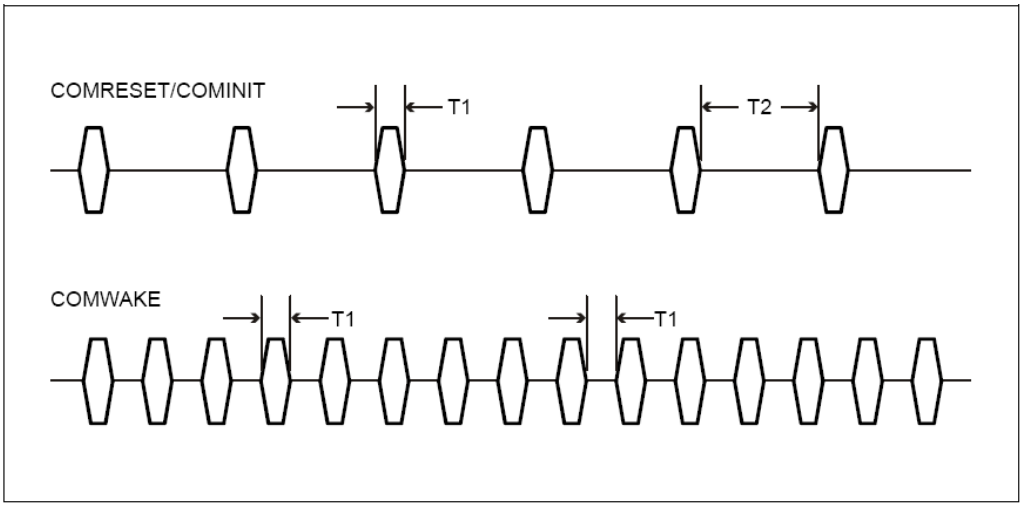

Figure 5: OOB signals

Table 9: *OOB signal times*

Time	Value
T1	160 UI_{oob} (106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

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3.4. *COMRESET*

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing.

The COMRESET signal shall be:

1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or 2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or 3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looks for four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 6 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.

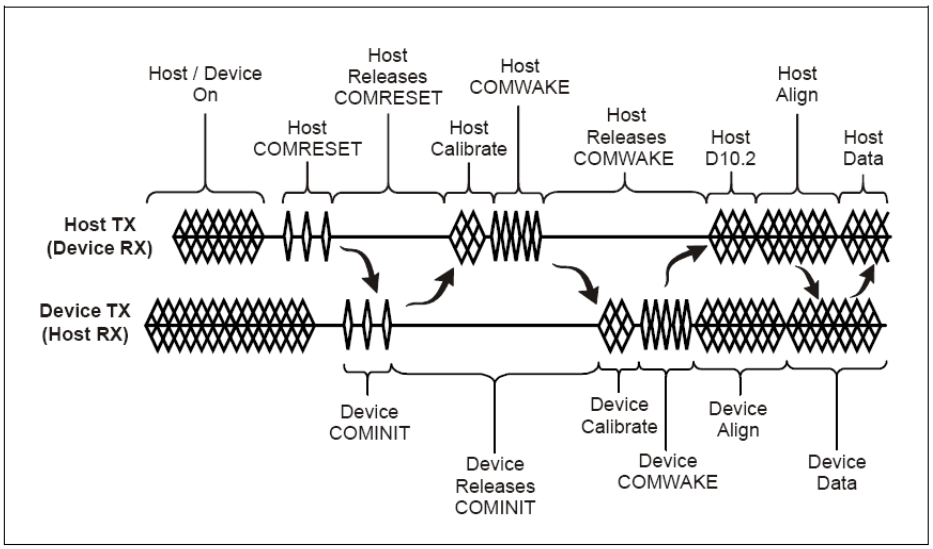

Figure 6: Comreset sequence

Description:

1). Host and device are powered and operating normally with some form of active communication.

2). Some condition in the host causes the host to issue COMRESET

3). Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.

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4). Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.

5). Host calibrates and issues a COMWAKE.

6). Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

7). Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.

8). Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

9). Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

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3.5. *COMINIT*

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 7, below:

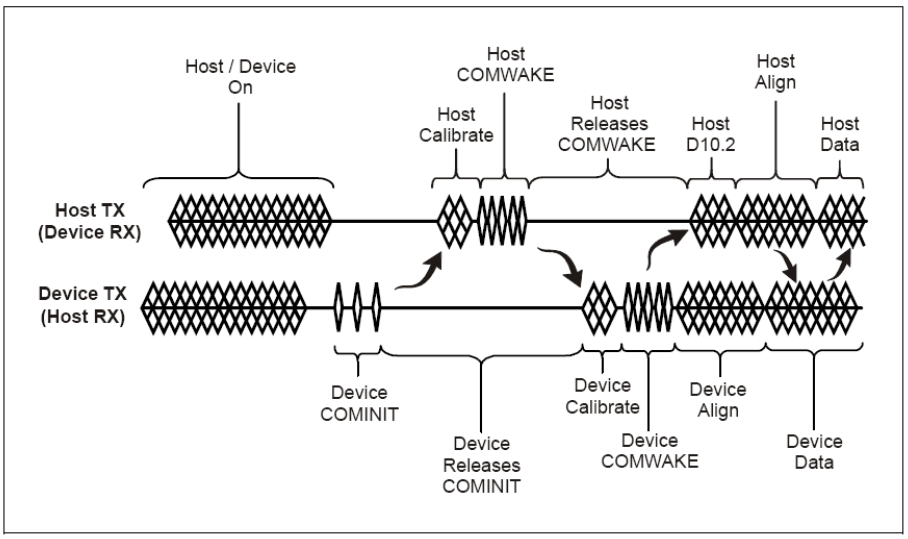

Figure 7: COMINIT sequence

Description:

1). Host / device are powered and operating normally with some form of active communication.

2). Some condition in the device causes the device to issues a COMINIT.

3). Host calibrates and issues a COMWAKE.

4). Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

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6). Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

7). Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

3.6. *Power on sequence timing diagram*

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 8.4 comprise the normative behavior specification and is the ultimate reference

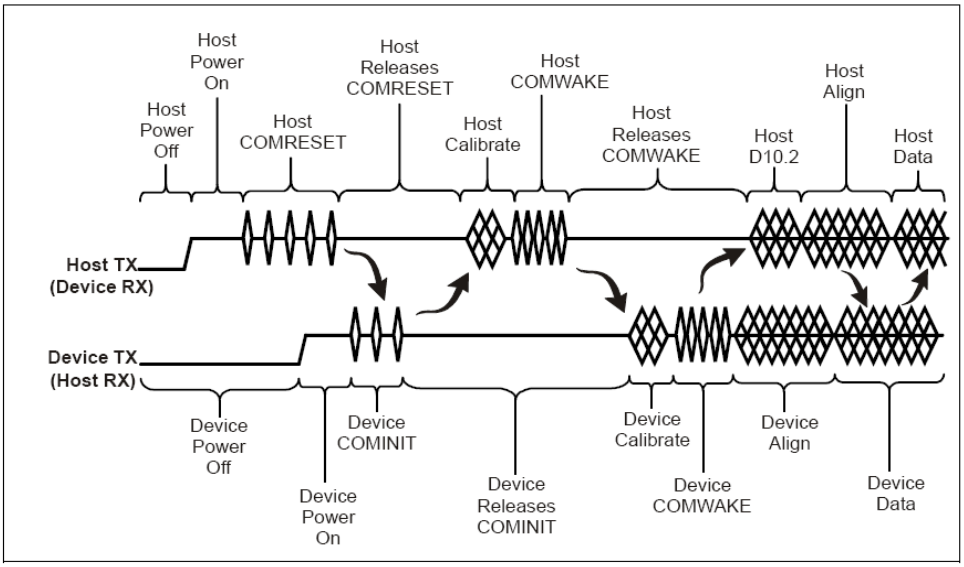

Figure 8: Power on sequence

Description:

1). Host/device power-off - Host and device power-off.

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2). Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).

3). Host issues COMRESET

4). Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.

5). Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.

6). Host calibrates and issues a COMWAKE.

7). Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.

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9). Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNCP primitive indicating it is ready to start normal operation.

10). Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

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4. Command Sets

4.1 ATA register

This table with the following paragraphs summarizes the ATA command set.

Table 10: Command table

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X

Notes:
O = Valid, X = Don't care
SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low/High Register
DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)
HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)
FT = Features Register

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4.2 ATA Command specifications

CHECK POWER MODE (E5h)

The host can use this command to determine the current power management mode.

EXECUTE DIAGNOSITICS (90h)

This command performs the internal diagnostic tests implemented by the drive. See ERROR register for diagnostic codes.

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Table 11: Identify device information default value

Word	Value	F/V	Description
0	0040h	 F X F X X F X F	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Reserved 1 Retired 0 Reserved
1	XXXXh	X	Number of logical cylinders
2	C837h	V	Specific configuration
3	00XXh	X	Number of logical heads
4-5	XXXXh	X	Retired
6	XXXXh	X	Number of logical sector per logical track
7-8	XXXXh	V	Reserved for assignment by the CompactFlash_ Association
9	000Eh	X	Retired
10-19	XXXXh	F	Serial number (20 ASCII characters)
20-21	XXXXh	X	Retired
22	003Fh	X	Obsolete
23-26	XXXXh	F	Firmware revision (8 ASCII characters)

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Word	Value	F/V	Description
27-46	XXXXh	F	Model number (40 ASCII characters)
47	8000h	F F F	15-8 80h 7-0 00h = Reserved 01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	4000h	F	Reserved
49	2F00h	 F F F F F F X	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired
50	4000h	 F F F X F	Capabilities 15 Shall be cleared to zero. 14 Shall be set to one. 13-2 Reserved. 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.
51	0280h	X	15-8 PIO data transfer cycle timing mode 7-0 Reserved
52	0000h	X	Obsolete
53	0007h	F F F X	15-3 Reserved 2 1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words 70:64 are valid 0 = the fields reported in words 70:64 are not valid 0 1 = the fields reported in words 58:54 are valid 0 = the fields reported in words 58:54 are not valid
54	XXXXh	X	Number of current cylinders
55	00XXh	X	Number of current heads
56	XXXXh	X	Number of current sector per track
57-58	XXXXh	X	Current capacity in sectors
59	0000h	F V V	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	F	Total number of user addressable sectors
62	0000h	X	Obsolete
63	0007h	F V 	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected

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Word	Value	F/V	Description
		V	9 1 = Multiword DMA mode 1 is selected
			0 = Multiword DMA mode 1 is not selected
		V	8 1 = Multiword DMA mode 0 is selected
			0 = Multiword DMA mode 0 is not selected
		F	7-3 Reserved
		F	2 1 = Multiword DMA mode 2 and below are supported
		F	1 1 = Multiword DMA mode 1 and below are supported
		F	0 1 = Multiword DMA mode 0 is supported
64	0003h	F	15-8 Reserved
		F	7-0 Advanced PIO modes supported
65	0078h	F	Minimum Multiword DMA transfer cycle time per word
66	0078h	F	Manufacturer's recommended Multiword DMA transfer cycle time
67	0078h	F	Minimum PIO transfer cycle time without flow control
68	0078h	F	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	F	Reserved (for future command overlap and queuing)
80	01FEh		Major version number 0000h or FFFFh = device does not report version
		F	15 Reserved
		F	14 Reserved for ATA/ATAPI-14
		F	13 Reserved for ATA/ATAPI-13
		F	12 Reserved for ATA/ATAPI-12
		F	11 Reserved for ATA/ATAPI-11
		F	10 Reserved for ATA/ATAPI-10
		F	9 Reserved for ATA/ATAPI-9
		F	8 Reserved for ATA/ATAPI-8
		F	7 1 = supports ATA/ATAPI-7
		F	6 1 = supports ATA/ATAPI-6
		F	5 1 = supports ATA/ATAPI-5
		F	4 1 = supports ATA/ATAPI-4
		F	3 Obsolete
		X	2 Obsolete
		X	1 Obsolete
		F	0 Reserved
81	0021h	F	Minor version number
82	0068h		Command set supported.
		X	15 Obsolete
		F	14 1 = NOP command supported
		F	13 1 = READ BUFFER command supported
		F	12 1 = WRITE BUFFER command supported
		X	11 Obsolete
		F	10 1 = Host Protected Area feature set supported
		F	9 1 = DEVICE RESET command supported
		F	8 1 = SERVICE interrupt supported
		F	7 1 = release interrupt supported
		F	6 1 = look-ahead supported

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Word	Value	F/V	Description
		F	5 1 = write cache supported
		F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3 1 = mandatory Power Management feature set supported
		F	2 1 = Removable Media feature set supported
		F	1 1 = Security Mode feature set supported
		F	0 1 = SMART feature set supported
83	5000h		Command sets supported.
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13-9 Reserved
		F	8 1 = SET MAX security extension supported
		F	7 Reserved
		F	6 1 = SET FEATURES subcommand required to spinup after power-up
		F	5 1 = Power-Up In Standby feature set supported
		F	4 1 = Removable Media Status Notification feature set supported
		F	3 1 = Advanced Power Management feature set supported
		F	2 1 = CFA feature set supported
		F	1 1 = READ/WRITE DMA QUEUED supported
		F	0 1 = DOWNLOAD MICROCODE command supported
84	4000h		Command set/feature supported extension.
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13-2 Reserved
		F	1 1 = SMART self-test supported
		F	0 1 = SMART error logging supported
85	0008h		Command set/feature enabled.
		X	15 Obsolete
		F	14 1 = NOP command enabled
		F	13 1 = READ BUFFER command enabled
		F	12 1 = WRITE BUFFER command enabled
		X	11 Obsolete
		V	10 1 = Host Protected Area feature set enabled
		F	9 1 = DEVICE RESET command enabled
		V	8 1 = SERVICE interrupt enabled
		V	7 1 = release interrupt enabled
		V	6 1 = look-ahead enabled
		V	5 1 = write cache enabled
		F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3 1 = Power Management feature set enabled
		F	2 1 = Removable Media feature set enabled
		V	1 1 = Security Mode feature set enabled
		V	0 1 = SMART feature set enabled

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Word	Value	F/V	Description
86	5000h	F	Command set/feature enabled.
		F	15-9 Reserved
		F	8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD
		F	7 See Address Offset Reserved Area Boot, INCITS TR27:2001
		V	6 1 = SET FEATURES subcommand required to spin-up after power-up
		V	5 1 = Power-Up In Standby feature set enabled
		V	4 1 = Removable Media Status Notification feature set enabled
		F	3-1 1 = Advanced Power Management feature set enabled
			0 1 = DOWNLOAD MICROCODE command supported
87	4000h		Command set/feature default.
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13-2 Reserved
		F	1 1 = SMART self-test supported
		F	0 1 = SMART error logging supported
88	203Fh		15-13 Reserved
		V	12 1 = Ultra DMA mode 4 is selected
			0 = Ultra DMA mode 4 is not selected
		V	11 1 = Ultra DMA mode 3 is selected
			0 = Ultra DMA mode 3 is not selected
		V	10 1 = Ultra DMA mode 2 is selected
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
		F	7-5 Reserved
		F	4 1 = Ultra DMA mode 4 and below are supported
		F	3 1 = Ultra DMA mode 3 and below are supported
		F	2 1 = Ultra DMA mode 2 and below are supported
		F	1 1 = Ultra DMA mode 1 and below are supported
		F	0 1 = Ultra DMA mode 0 is supported
89	0000h	F	Time required for security erase unit completion
90	0000h	F	Time required for Enhanced security erase completion
91	0000h	V	Current advanced power management value
92	0000h	V	Master Password Revision Code
93	0000h	X	Hardware reset result
94-126	0000h	V	Reserved
127	0000h	F	Removable Media Status Notification feature set support
		F	15-2 Reserved
			1-0 00 = Removable Media Status Notification feature set not supported
			01 = Removable Media Status Notification feature supported
			10 = Reserved
			11 = Reserved

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Word	Value	F/V	Description
128	0001h		Security status
		F	15-9 Reserved
		V	8 Security level 0 = High, 1 = Maximum
		F	7-6 Reserved
		F	5 1 = Enhanced security erase supported
		V	4 1 = Security count expired
		V	3 1 = Security frozen
		V	2 1 = Security locked
		V	1 1 = Security enabled
		F	0 1 = Security supported
129-159	0000h	X	Vendor specific
160-254	0000h	X	Reserved
255	0000h	X	Integrity word 15-8 Checksum 7-0 Signature
Key: F/V = Fixed/variable content F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed. V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device. X = the content of the word may be fixed or variable.			

IDLE (E3h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

INITIALIZE DEVICE PARAMETERS (91h)

This command enables the host to set the number of sectors per track and the number of tracks per heads.

READ DMA (C8h)

Reads data is from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h/21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector

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number register. A sector counts of the requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

RECALIBRATE (10h)

The current drive performs no processing if it receives this command. It is supported for backward compatibility with previous devices.

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock.

The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

• SECURITY SET PASSWORD
• SECURITY UNLOCK
• SECURITY DISABLE PASSWORD
• SECURITY ERASE PREPARE
• SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued

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when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

SECURITY UNLOCK (F2h)

This command disabled LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

SEEK (7xh)

This command is effectively a NOP command to the device although it does perform a range check.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

Table 12: Features register value and settable operating mode

Value	Value Function
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register.
55h	Disable read look-ahead feature
82h	Disable write cache
AAh	Enable read look-ahead feature

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

SLEEP (E6h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

SMART Function Set (B0h)

Performs different processing required for predicting device failures, according to the subcommand specified in the Features register. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

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STANDBY (E2h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h/31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

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5. Electrical Specification

5.1. Absolute Maximum Rating

Table 13: Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Analog power supply	AVDDH		-0.5	6	V
Digital I/O power supply	DVDD		-0.5	6	V
Digital I/O input voltage	VI(D)		-0.4	DVDD+0.4	V
Storage temperature	TSTORAGE		-55	140	°C

5.2. Recommended Power Supply Operation Condition and Temperature

Table 14: Recommended Power Supply Operation Conditions and Temperature

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Operation digital power supply	PV33		3.0	3.3	3.6	V
	D1V2		-5%	1.2	+5%	V
Operation analog power supply	ASV33		3.0	3.3	3.6	V
	ASV12		-5%	1.2	+5%	V
	AVDDH		3.0	3.3	3.6	V
Operation DDR_PP power supply	DDR_PP		1.7	1.8	1.9	V
Operation DDR_Vref power supply	DDR_VREF	Vref=0.5x DDR_PP	0.85	Vref	0.95	V
Ambient operation temperature	TA	For commercial spec.	0		70	°C
Ambient operation temperature	TA	For industry spec.	-40		85	°C
Junction temperature	TJ				125	°C
Case operation temperature	Tc	For commercial spec and base on TA			85	°C
Case operation temperature	Tc	For industry spec and base on TA			100	°C
TFBGA ?ball	θJC					°C/W
TFBGA ?ball	θJA					°C/W

5.3. Recommended External Clock Source Conditions

Table 15: Recommended External Clock Source Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				30		MHz
Clock Duty Cycle			45	50	55	%

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5.4. *Power Supply DC Characteristics*

Table 16: Power Supply DC Characteristics

Power supply: PC's SATA 5V input.					(Max=Peak)	
Parameter	**Symbol**	**Condition**	**Min**	**Typical**	**Max**	**Unit**
Digital Power Supply	IPV33	3.3V		7	14	mA
	IDV12	1.2V		272	373	mA
USB Analog Power Supply	IAVDDH	3.3V		6	18	mA
SATA Analog Power Supply	IASV33	3.3V		34	41	mA
SATA Analog Power Supply	IASV12	1.2V		61	68	mA
DDR PAD and DDRII	IDDR_PP	1.8V		143	162	mA

Note: SATA Idle mode and power saving mode are disabled.

5.5. *Power Supply DC Characteristics (SATA Active mode)*

Table 17: Power Supply DC Characteristics

Power supply: PC's SATA 5V input.					(Max=Peak)	
Parameter	**Symbol**	**Condition**	**Min**	**Typical**	**Max**	**Unit**
Digital Power Supply	IPV33	3.3V		44	103	mA
	IDV12	1.2V		320	442	mA
USB Analog Power Supply	IAVDDH	3.3V		6	18	mA
SATA Analog Power Supply SATA	IASV33	3.3V		34	41	mA
Analog Power Supply	IASV12	1.2V		61	67	mA
DDR PAD and DDRII	IDDR_PP	1.8V		135	302	mA

5.6. *I/O DC Characteristics*

Table 18: I/O DC Characteristics

Parameter	**Symbol**	**Condition**	**Min**	**Typical**	**Max**	**Unit**
Input low voltage	VIL				0.8	V
Input high voltage	VIH		2.4			V
Output low voltage	VOL		1.5			V
Output high voltage	VOH				3.3	V

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Appendix A: Ordering Information

1. Part Number List

◆ **APRO Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series**

Grade	*Standard grade (0ºC ~ 70ºC)*	*Industrial grade (-40ºC ~ +85ºC)*
16GB	SR2SR016G-JDCMC	WR2SR016G-JDCMC/C
32GB	SR2SR032G-JDCMC	WR2SR032G-JDCMC/C
64GB	SR2SR064G-JDCMC	WR2SR064G-JDCMC/C
128GB	SR2SR128G-JDCMC	WR2SR128G-JDCMC/C
256GB	SR2SR256G-JDCMC	WR2SR256G-JDCMC/C

Notes: */C stands Special conformal coating treated on whole PCBA which may support industrial grade operating temperature -40°C ~ +85°C*

2. Part Number Decoder

X1 X2 X3 X4 X5 X6 X7 X8 X9 — X11 X12 X13 X14 X15 / C

X1 : **Grade**

S: Standard Grade – operating temp. 0º C ~ 70 º C

W: Industrial Grade- operating tem. -40º C ~ +85 º C

(Commercial grade with conformal coating)

X2 : **The material of case**

R : 2.5" Rugged Metal Casing

X3 X4 X5 : **Product category**

2SR : 2.5" SATA II SSD HERMES Series R version supports DDRII SDRAM 512Mbit cache

X6 X7 X8 X9 : **Capacity**

016G:	16GB	**128G:**	128GB
032G:	32GB	**256G:**	256GB
064G:	64GB		

X11 : **Controller**

J : JMicron (HERMES-R Series)

X12 : Controller version

A, B, C, D…

X13 : **Controller Grade**

C : Commercial grade

X14 : **Flash IC**

M : MLC-NAND Flash IC

X15 : **Flash IC grade / Type**

C : Commercial grade

C : **Reserved for specific requirement**

C : Conformal-coating

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Appendix B: Limited Warranty

APRO warrants your Rugged Metal 2.5" SATA II MLC SSD HERMES-R Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **SR2SRxxxG-JDCMC** **1 year**
- **WR2SRxxxG-JDCMC/C** **1 year**

The warranty period is able to extend. Please contact APRO and/or Your APRO distributors for more information.

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